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CPLD/FPGA BOARDS

FPGA SPARTAN 3 an Evaluation Kit

USER MANUAL

Contents

1. Introduction 3
   1.1– Packages 3
   1.2- Technical or Customer Support 3
2. Key Components and Features 3
   2.1- General Block Diagram 4
3. Jumper & Switch Details 5
4. Connector Details 6
5. Power Supply 7
6. On-board Peripherals 7
   6.1 - Light Emitting Diodes 8
   6.2 – Digital Inputs 9
   6.3 – 2x16 Char LCD Display 10
   6.4 – 5x1 Matrix keypad 11
   6.5 - DC Motor .....
   6.6 – Buzzer Interface .....
   6.7 –12 Bit SPI ADC .....
   6.8 –12 Bit SPI DAC .....

7 - Peripherals Section - II 13
   7.1 - RS-232 Communication(USART) 13
   7.2 – Clock Source 14
   7.3 – JTAG Programmer 14

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1. *Introduction*

The intention of the design is to endorse the engineers and scholars to exercise and explore the capabilities of FPGA architectures with many interfacing modules on board point LEDs, Slide switches, LCD, ADC, DAC, Buzzer, UART and Push Buttons with ease to create a stand-alone versatile test platform.

1.1– Packages

- Spartan-3AN Evaluation Kit (XC3S50AN)
- Serial Port Cable
- JTAG Programming Cable
- Printed User Manual
- CD contains
  - Software (Programmers, ISE)
  - Example Programs
  - User Manual

1.2 - Technical or Customer Support

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2. *Key Components and Features*

On-Chip Features

- 50,000-gate Xilinx Spartan 3AN FPGA in a 144-TQG (XC3S50-4TQG144C)

- 1,584 logic cell equivalents
- 54K-bit block RAMs
- Three 18x18 hardware multipliers
- Two Digital Clock Managers (DCMs)
- Up to 108 user-defined I/O signals

On-Board Features

- 8 Nos. Slide Switches for digital inputs
- 8 nos. of Point LEDs for Digital outputs
- 2x16 Character LCD interface
- 5x1 Matrix Keypad interface
- RS-232 Serial Port.
- 12-Bit SPI ADC
- 12-Bit SPI DAC
- Buzzer
- 50 MHz crystal oscillator clock source
- 40-pin I/O connector for interface external peripherals modules
- JTAG port for download user program through cable
- 9V AC/DC power input through adapter
- On-board 5V, 3.3V and 1.2V regulators.

2.1- General Block Diagram

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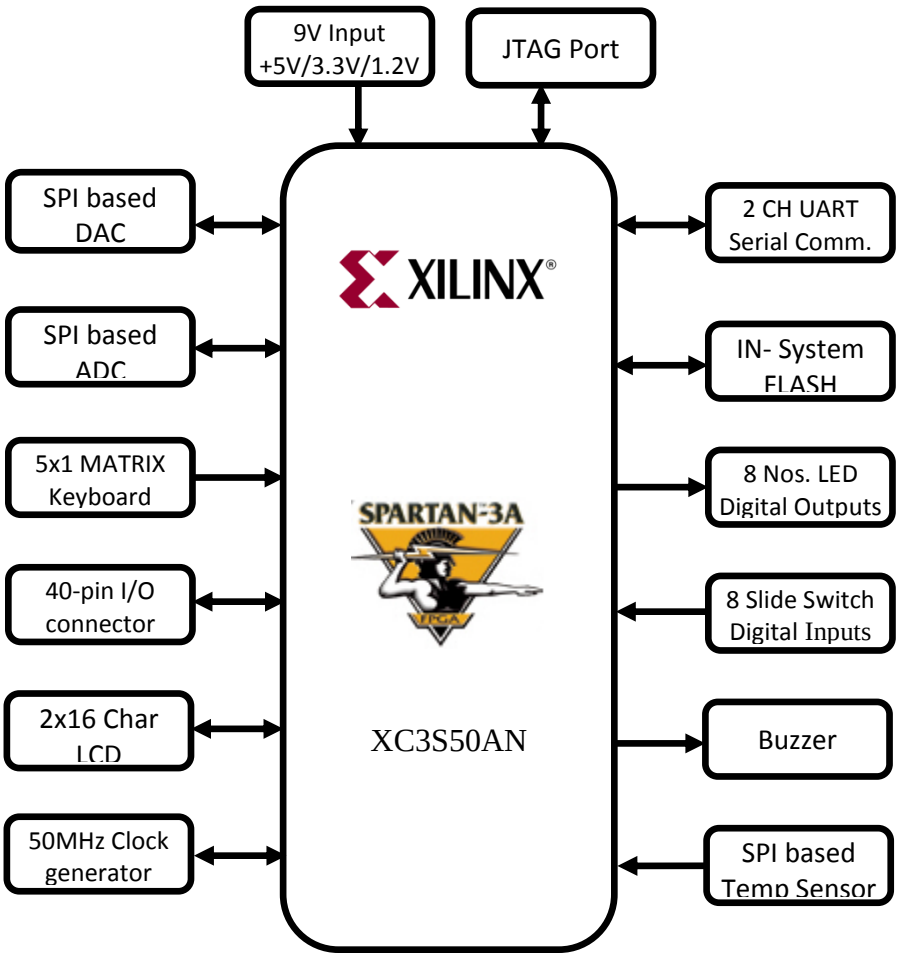
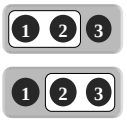
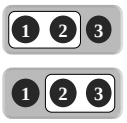


3. *Jumper & Switch Details*

ADC External Input **JP1**		External Input to CH1 External Input to CH0
ADC Channel 0 **JP2**		Internal Trim Pot Input External Input
ADC Channel 1 **JP3**		Internal Temperature Sensor Input External Input

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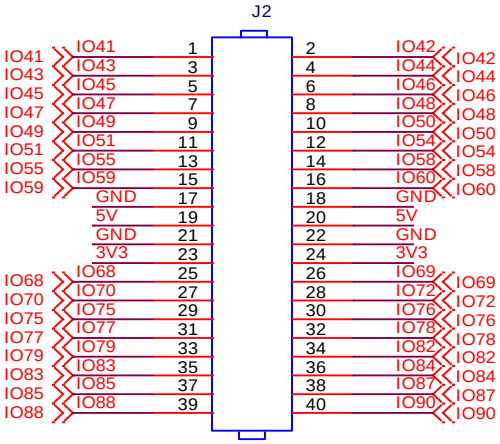
Buzzer **J5**		Enable Buzzer Disable Buzzer

Program Execution Mode Selection (EXE MODE)		
JTAG/FLASH **J3**	M0 M1 M2 	MODE1- JTAG Programming MODE2- Flash Programming

4. *Connector Details*

40pin – Box Connector



JTAG Connector

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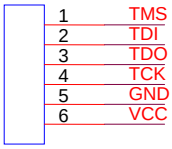

5. *Power Supply*

The external power can be AC or DC, with a voltage between (9V, 1A output) at 230V AC input. The SPARTAN3AN board produces +5V using an LM7805 voltage regulator, which provides supply to the peripherals.

Separate **On/Off** Switch (SW1) for controlling power to the board.

ON/OFF SW2		Power +5V ***ON*** -External through ***Adaptor*** Power +0V ***OFF***

There are multiple voltages supplied on the Spartan-3AN Evaluation Kit, 3.3V and 1.2V regulators. Similarly, the 3.3V regulator feeds all the VCCO voltage supply inputs to the FPGA's I/O banks and powers most of the components on the board.

The FPGA configuration interface on the board is powered by 3.3V. Finally, a 1.2V regulator supplies power to the FPGA's VCCINT voltage inputs, which power the FPGA's core logic. The board uses three discrete regulators to generate the necessary voltages.

6. *On-board Peripherals*

The Development Kit comes with many interfacing options

- 8 Nos. Slide Switches for digital inputs
- 8 nos. of Point LEDs for Digital outputs
- 2x16 Character LCD interface

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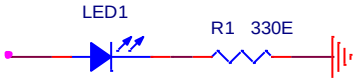
- 5x1 Matrix Keypad interface
- Buzzer Interface
- Clock Source
- 12-Bit SPI ADC
- 12-Bit SPI DAC
- Buzzer
- JTAG Programmer
- UART for serial port communication through PC

6.1 - Light Emitting Diodes

- Light Emitting Diodes (LEDs) are the most commonly used components, usually for displaying pin's digital states.

- The FPGASP3 KIT has 8 nos., of Point LEDs, connected with port pins (details tabulated below); the cathode of each LED connects to ground via a 330Ω resistor. To light an individual LED, drive the associated FPGA control signal to **High.**

	Point LEDs	XC3S200 - Pins	LED Selection
DIGITAL OUTPUTS	LED-LD1	P7	 Make Pin High – LED ON Make Pin Low – LED OFF
	LED-LD2	P8	
	LED-LD3	P10	
	LED-LD4	P11	
	LED-LD5	P12	
	LED-LD6	P13	
	LED-LD7	P15	
	LED-LD8	P16	

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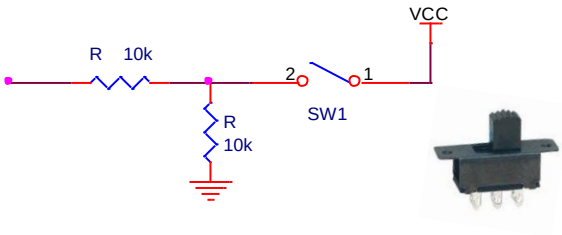
6.2 – Digital Inputs

- This is another simple interface, of 8-Nos. of slide switch, mainly used to give an input to the port lines, and for some control applications also.

- The FPGASP3AN KIT, slide switches (SW7-SW14) directly connected with FPGA I/O lines (details tabulated below), user can give logical inputs **high** through slide switches.

The switches are connected to +3.3V, in order to detect a switch state, by default lines are pull-downed through resistors. The switches typically exhibit about 2 ms of mechanical bounce and there is no active de-bouncing circuitry, although such circuitry could easily be added to the FPGA design programmed on the board. A 10KΩ series resistor provides nominal input protection.

	Slide Switch	XC3S200 - Pins	Slide Switch Logic
DIGITAL INTPUTS	SW7	P18	 Make Switch Close – High Make Switch Open – Low
	SW8	P19	
	SW9	P20	
	SW10	P21	
	SW11	P24	
	SW12	P25	
	SW13	P27	
	SW14	P28	

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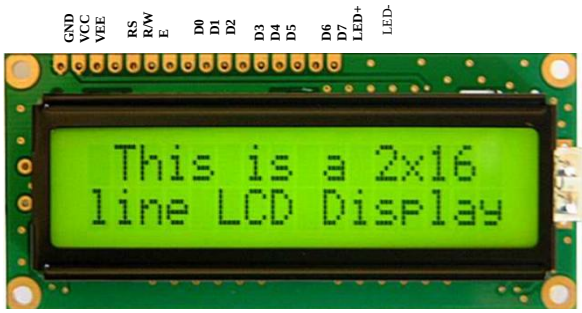
6.3 – 2x16 Char LCD Display

The 2x16 character LCD interface card with supports both modes 4-bit and 8-bit interface, and also facility to adjust contrast through trim pot. In 8-bit interface 11 lines needed to create 8-bit interface; 8 data bits (D0 – D7), three control lines, address bit (RS), read/write bit (R/W) and control signal (E). The LCD controller is a standard KS0070B or equivalent, which is a very well-known interface for smaller character based LCDs.

	LCD MODULE	XC3S200-Pins	2x16 LCD Selection
CONTRO	RS	P105	
	RW	P104	
	E	P103	
DATA LINES	D0	P102	
	D1	P101	
	D2	P99	
	D3	P98	
	D4	P96	
	D5	P93	
	D6	P92	
	D7	P91	

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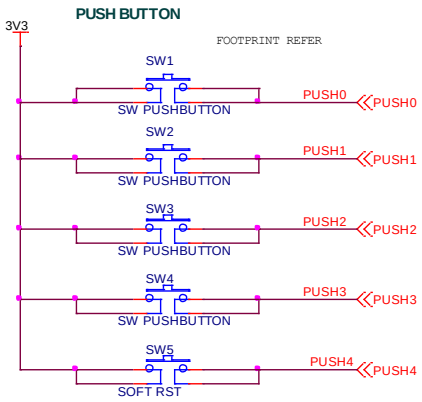
6.5 - 5x1 Matrix keypad

Keypads arranged by matrix format, each row and column section pulled by high, all row lines and column lines connected directly by the I/O pins.

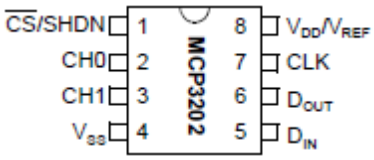
5X1Matrix Keys	XC3S50AN-pins	Matrix Format
PUSH BUTTON-SW1	P29	
PUSH BUTTON-SW2	P30	
PUSH BUTTON-SW3	P31	
PUSH BUTTON-SW4	P32	
PUSH BUTTON-SW5	P33	

6.6 – 12 Bit ADC

These ADCs are SPI Bus based which is a serial bus. So the number of pins in IC is very low. Total of 4 lines are required to interface it with FPGA.

1. MISO (Master In Slave Out)
2. MOSI (Master Out Slave In)
3. SCK (Serial Clock)
4. CS (Chip Select)

2 CHANNEL ADC



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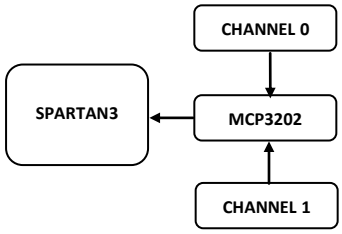
ADC PIN	SPARTAN3AN FPGA Lines	ADC CHANNEL SELECTION
DOUT	P114	
DIN	P113	
SCK	P111	
CS	P110	

As you know in synchronous serial communication their is a clock line (SCK in case of SPI) which synchronizes the transfer.

The clock is always controlled by the MASTER. In our case the Spartan3AN is the MASTER and the MCP3202 is a slave on the bus. SPI is full duplex, that means data can be sent and received simultaneously.

SPI Transfer.

A SPI transfer is initiated by the MASTER pulling the CS line low. The CS line sits at HIGH during idle state. Now master can write to the bus in 8bit (or 1 byte) chunks. One most important thing to note about SPI is that for every byte MASTER writes to SLAVE the MASTER receives one byte in return. So the only transaction possible is exchange of data. Their is no separate Read and Write commands their is only one command and that is Write.

6.7 – 12 Bit SPI DAC

The controller designed coverts the digital data into analog, where the digital data is transferred using SPI Controller and DAC (MCP4921) converts the serial data into the analog. SPI Controller controls the speed, data transmission, DAC selection etc. Based on the inputs from the SPI line, DAC (MCP4921) coverts the 12 bit data to analog.

SPI DAC

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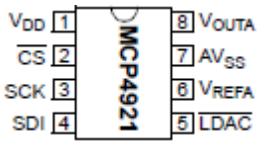

DAC PIN	SPARTAN3AN FPGA Lines	DAC SELECTION
CS	P58	SPARTAN3 → MCP4921 → ANALOG O/P
SCK	P59	
SDI	P60	

6.9 – Buzzer Interface

5V continuous buzzer connected through FPGA's I/O pins (P5), to enable buzzer place jumper JP7 at E label mark position.

Buzzer Module **:** Spartan3 FPGA pins (Buzzer – P5), make port pins to high, buzzer will activated

	5V Buzzer	XC3S50AN-pins	RELAY Power Select
Buzzer	Buzzer	P64	J5 (1 2 3) To Enable Buzzer

7 - Peripherals Section - II

7.1 - RS-232 Communication(USART)

USART stands for Universal Synchronous Asynchronous Receiver Transmitter. FPGASP3AN Kit provides an RS232 port that can be driven by the Spartan-3AN FPGA. A subset of the RS232 signals is used on the Spartan 3AN kit to implement this interface (RxD and TxD signals).

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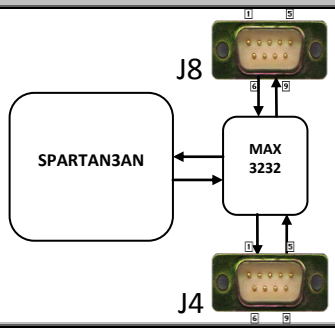
- RS-232 communication enables point-to-point data transfer. It is commonly used in data acquisition applications, for the transfer of data between the microcontroller/FPGA and a PC.

- The voltage levels of a FPGA and PC are not directly compatible with those of RS-232, a level transition buffer such as MAX3232 be used.

	UART DB-9 Connector	SPARTAN3AN FPGA Lines	Serial Port Section
UART	TXD0	P3	
	TXD1	P4	
	RXD0	P5	
	RXD1	P6	

7.2 – Clock Source

The FPGASP3 Kit has a dedicated 50 MHz series clock oscillator source and an optional socket for another clock oscillator source.

	U18	Signal	SPARTAN3 FPGA Lines	Crystal Oscillator
Oscillator	50MHz	Clock	P57	

7.3 – JTAG Programmer

The FPGASP3 Kit includes a JTAG programming and debugging chain. Pantech JTAG3 low-cost parallel to JTAG cable is included as part of the kit and connects to the JTAG header. DB-25 parallel port connector to 6 pin female header connector. The JTAG cable connect directly to the parallel port of a PC and to a standard 6 pin JTAG programming header in the kit, can program a devices that have a JTAG voltage of 1.8V or greater.

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	6-Pin Header	JTAG Signals	SPARTAN3 FPGA Lines	JTAG Cable – III
JTAG Programmer	1	TMS	P1	
	2	TDI	P2	
	3	TDO	P107	
	4	TCK	P109	
	5	GND		
	6	VCC		

The Pantech low-cost parallel port to JTAG cable fits directly over the header stake pins, as shown in above figure. When properly fitted, the cable is perpendicular to the board. Make sure that the signals at the end of the JTAG cable align with the labels listed on the board. The other end of the Pantech cable connects to the PC's parallel port. The Pantech cable is directly compatible with the Xilinx iMPACT software.

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